

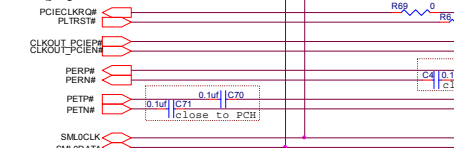
Intel® I219 Reference Schematic

February 2015 – Rev1.0

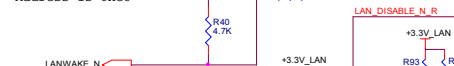
Copyright© Intel Corporation, 2015

DESIGN NOTE: Not all PCH's PCIe ports can be used for LAN device. See Platform Design Guide for what PCIe ports can be used with the LAN device.

DESIGN NOTE: i219's CLK_REQ_N must be connected to PCH's CLKREQ# pin.



NOTE: Default SMBus Address is 0xC8



DESIGN NOTE: LAN_WAKE_N must be connected to PCH's LAN_WAKE input.

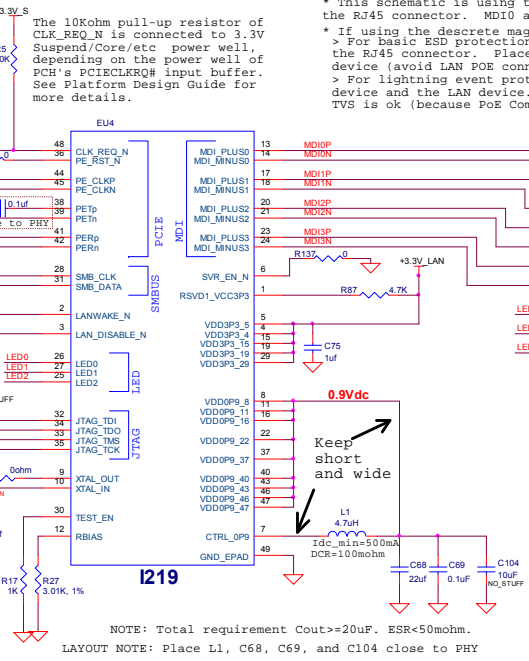


DESIGN NOTE: LAN_DISABLE_N must be connected to PCH's GPIO/LANPHYPC output. This GPIO pin must be set as "LANPHYPC" function through FITO tool. The signal does not require pull-up. R15 resistor is no-stuff default (for testing purpose).

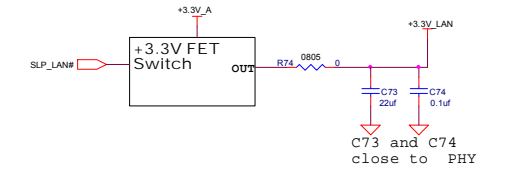
CRYSTAL DESIGN NOTE: I219 supports crystal parts with Cload=18pF. Using formula, Cload=[(C7*C8)/(C7+C8)]+Cstray. C7/C8 value is depending on the actual Cstray of the board. Cstray is varied based on specific board stack-up, layout, etc. If Cstray=9pF, then select C7=C8=19pF. If Cstray=7pF, then select C7=C8=22pF. If Cstray=5pF, then select C7=C8=27pF. Since most boards have Cstray=7pF, select C7=C8=22pF is a good default value. I219 is also tested with few Crystals which has Cload=10pF. When using these Cload=10pF Crystals, select C7=C8=10pF. Please see the i219 datasheet for the evaluated parts list. Each design must measure the crystal's PPM frequency accuracy.

REVISION HISTORY

Rev	Notes
0.5	1st release (based I218 Reference Schematic). Update design notes
0.7	Add Design Note for PCIe port selection. Add Design Note for LED pins. Updated Power Supply Notes.
1.0	Updated Crystals, Power, and TVS Design Notes.

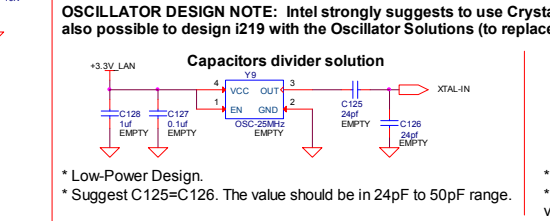
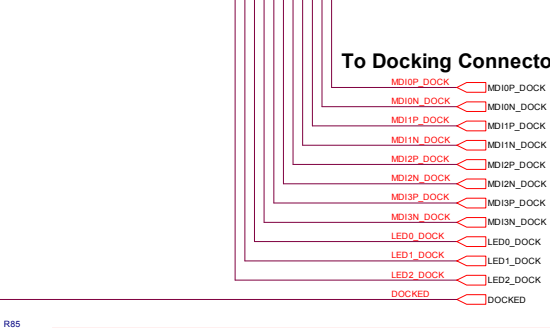
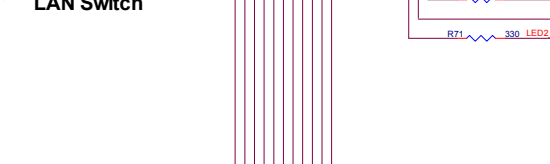
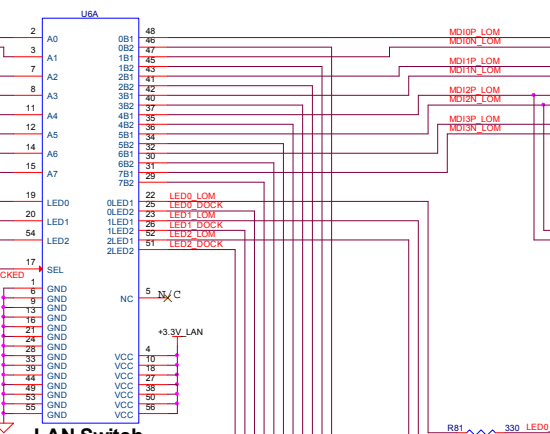


NOTE: Total requirement Cout=20uF. ESR<50mohm.
LAYOUT NOTE: Place L1, C68, C69, and C104 close to PHY

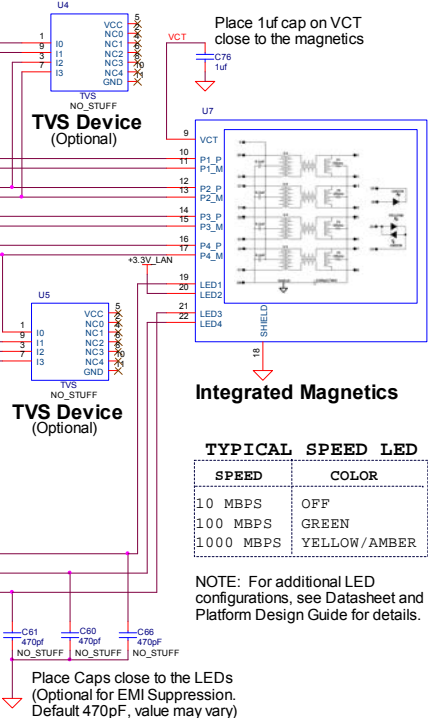


POWER SUPPLY NOTES: +3.3V_A is always on during G3->S5, S0, Sx, and DeepSx states.
PCH's SLP_LAN# output pin is the ONLY control signal which can be used for gating the i219 power. If PCH's SLP_LAN# is not used, i219 should always have power during all networking conditions (S0, Sx, WOL, etc.)

TVS DESIGN NOTES:
* This schematic is using the integrated magnetics RJ45 connector. Place TVS devices close to the RJ45 connector. MDI0 and MDI1 pairing on a same TVS is ok (no PoE connecting issue).
* If using the discrete magnetics device:
> For basic ESD protection (IEC61000-4-2), place the TVS devices between the magnetics device and the RJ45 connector. Place it close to the RJ45 connector. Do not pair MDI0 and MDI1 on a same TVS device (avoid LAN PoE connecting issue). MDI0 can pair with either MDI2 or MDI3 on a same TVS.
> For lightning event protection (IEC61000-4-5), place the TVS devices between the magnetics device and the LAN device. Place it close to the magnetics device. MDI0 and MDI1 pairing on a same TVS is ok (because PoE Common-Mode energy should not pass through the magnetics device).



OSCILLATOR DESIGN NOTE: Intel strongly suggests to use Crystal Circuit for i219 (widely use and low cost). However, it is also possible to design i219 with the Oscillator Solutions (to replace the Crystal Circuit). Below is 2 tested solutions.
* Low-Power Design.
* Suggest C125=C126. The value should be in 24pF to 50pF range.
* High-Power Design (due to current path through resistor R152).
* Suggest R151=R152. 100ohm is a good starting value. Higher value may cause violation of the rise/fall timing requirements.



DESIGN NOTE: The LED pins should only be used for LAN's LED purposes. In ULP mode, LAN's LED pins will be un-powered and might affect other logics (if these LED signals are connected to other logics).
NOTE: For additional LED configurations, see Datasheet and Platform Design Guide for details.

TYPICAL SPEED LED

SPEED	COLOR
10 MBPS	OFF
100 MBPS	GREEN
1000 MBPS	YELLOW/AMBER

NOTE: This is a typical Mobile Docking Design. For designs without a docking connector, the lanswitch device is not necessary so it can be removed. Please see the schematic/layout checklist for details.